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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,680	07/28/2004	Brent A. Anderson	BUR920040049US1	4309

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,680	ANDERSON ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 29-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 29-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 06/01/2006, claims 1-14 and 29-37 are active in this application.

Claim(s) 15-28 have been cancelled.

Claims 29-37 are newly added claims.

Examiner's Amendment

2. The following amendments have been made to the claim(s) to correct the clerical error since there are two different claims 31 in the currently pending claim. Should the changes be unacceptable to applicant, an amendment may be filed during the subsequent communication(s).

Claims 31 to claim 37 have been renumbered as follow:

Pending claims		Renumbered claims
31	→	31
31	→	32
32	→	33
33	→	34
34	→	35
35	→	36

36 → 37

37 → 38

Remarks

3. Applicant's argument(s), filed 06/01/2006 have been fully considered, but are not persuasive.

First, with regard to the teaching of She et al. (US 2005/0242391), Examiner do/does not agree with Applicant that She neither teaches a logic gate adjacent a first of the channel nor the floating gate adjacent the second side of the channel. As described in paras. [0031] and [0035], and also asserted by Applicant, She discloses a trapping layer that functions as a nitride trap storage site. A floating gate is a charge trapping layer which holds charge(s) to influence the operation of the device (for further information about floating gate, see the online Wikipedia, the free encyclopedia at http://en.wikipedia.org/wiki/Floating_gate_transistor. In addition, fig. 11, for example, shows a channel region between the source and drain regions. A first gate structure, that is the lower gate structure having Gate 1, and a second gate structure, that is the upper gate structure having Gate 2, are formed on the opposite sides of the channel. The lower gate structure having Gate 1 is (considered as) a logic gate (for its ability to control the operation of the transistor), and is formed adjacent a first side which is the lower side of the channel. The upper gate structure having Gate 2 comprises a charge trapping layer, or a floating gate, which traps two charges, or two bits, Bit 1 and Bit 2

(note that the charge trapping layer where Bit 1 and Bit 2 are stored is the floating gate; Bit 1 and Bit 2 themselves are not gates, they are charges stored in the gate). The charge trapping layer, or the floating gate, where Bit 1 and Bit 2 are trapped, is formed adjacent to a second side which is the upper side of the channel. The first side is opposite to the second side, with respect to the channel region. The upper gate structure having Gate 2 also comprises a control gate, or a programming gate, which is formed adjacent to the floating gate or charge trapping layer. A tunnel oxide layer is formed between the channel and the floating gate; and a control oxide layer is formed between the floating gate and the programming gate. Clearly, She does teach all of the argued limitations.

Second, with regard to the teaching of Hsu (US 6,107,141), Applicant's arguments are not persuasive. Fig. 1 of Hsu, for example, shows a channel region, which is the surface region of the substrate 10 between drain region 20 and source region 30. The channel region has a first side which is the left side, or the source side, (or left portion, directly under gate 120) adjacent the source 30, and a second side which is the right side, or the drain side, (or right portion, right under gate 130) adjacent the drain 20. The first (source) side is opposite to the second (drain) side, with respect to the vertical oxide layer 231 (or with respect to a line vertically goes through the oxide layer 231). The select or logic gate 120 is adjacent the first (source) side of the channel region, and the floating gate is adjacent the second (drain) side of the channel region. A programming gate 140 is adjacent the floating gate 130, wherein the floating gate is

between the programming gate and the channel region. Oxide layer 232 is on the first (source) side of the channel region and is disposed between the logic gate 120 and the channel region. A tunnel oxide layer 235 is on the second (drain) side of the channel region and is disposed between the channel region and the floating gate 130. Clearly, Hsu does teach all of the argued limitations.

For the above reasons, the rejection in the last Office Action is believed to be proper and is included herewith, along with rejection to the newly added claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim(s) 1, 5, 6, 8, 12, 13, 29, 32, 34, 35, 37, and 38 stand rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent Application Publication No. 2005/0242391 by She et al.

Regarding claim 1, She discloses a multiple-gate transistor, as shown in figs. 10-11, comprising:

a channel region (between source and drain regions);

a logic gate (lower gate structure having Gate 1) adjacent a first side (lower side) of said channel region;

a floating gate (trapping layer, where Bit 1 and Bit 2 are trapped) adjacent a second side (upper side) of said channel region, wherein said first side is opposite said second side; and

a programming gate (control gate 2 formed on the control oxide and having dark region) adjacent said floating gate, wherein said floating gate is between said programming gate and said channel region.

Regarding claim 8, She discloses a multiple-gate transistor, as shown in figs. 10-11, comprising:

a channel region; source and drain regions at ends of said channel region;

a gate oxide (tunnel oxide) on a first side (lower side) of said channel region;

a logic gate (lower gate structure having Gate 1) adjacent said first gate oxide, wherein said gate oxide is between said logic gate and said channel region;

a first insulator (between channel region and the region where Bit 1 and Bit 2 being trapped) on a second side (upper side) of said channel region, wherein said second side of said channel region is opposite said first side;

a floating gate (trapping layer, where Bit 1 and Bit 2 are trapped) adjacent said first insulator wherein said first insulator is between said floating gate and said channel region;

a second insulator (Control oxide, between the trapping layer and gate 2 with dark region) adjacent said floating gate; and

a programming gate (control gate 2 formed on the control oxide and having dark region) adjacent said second insulator wherein said second insulator is between said programming gate and said floating gate.

Regarding claims 5, and 12, She discloses the transistor wherein said transistor comprises a fin-type field effect transistor (FinFET). See figs. 8-11.

Regarding claims 6, and 13, She discloses the transistor further comprising source and drain regions at ends of said channel region, wherein said channel region comprises the middle portion of a fin structure and said source and drain regions comprise end portions of said fin structure. See figs. 8-11.

Regarding claim 29, She discloses a multiple-gate transistor, as shown in figs. 10-11, comprising:

a channel region (between source/drain regions);

a logic gate (lower gate structure having Gate 1) adjacent a first side (lower side) of said channel, wherein voltage in said logic gate causes said transistor to switch on

and off (it is inherent that channel current, or the on/off state of a transistor can be controlled by voltage applied to the gate of the transistor);

a floating gate (trapping layer, where Bit 1 and Bit 2 are trapped) adjacent a second side (upper side) of said channel region, wherein said first side is opposite said second side, and wherein charge (Bit 1 and Bit 2) in said floating gate adjusts the threshold voltage of said transistors (this is inherent characteristics of floating gate transistor); and

a programming gate (control gate 2 formed on the control oxide and having dark region) adjacent said floating gate, wherein said floating gate is between said programming gate and said channel region.

Regarding claim 32, She discloses the transistor wherein said transistor comprises a fin-type field effect transistor (FinFET). See fig. 8-11.

Regarding claim 34, She discloses the transistor wherein said floating gate is electrically insulated from other structures. See figs. 10-11.

Regarding claim 35, She discloses a multiple-gate transistor, as shown in figs. 10-11, comprising:

a channel region (between source/drain regions);

a logic gate (lower gate structure having Gate 1) adjacent a first side (lower side) of said channel region, wherein voltage in said logic gate causes said transistor to

switch on and off (it is inherent that channel current, or the on/off state of a transistor can be controlled by voltage applied to the gate of the transistor), and wherein said transistor comprises a fin-type field effect transistor (FinFET) (see fig. 8-11);

a floating gate (trapping layer, where Bit 1 and Bit 2 are trapped) adjacent a second side (upper side) of said channel region, wherein said first side is opposite said second side, and wherein charge in said floating gate adjusts the threshold voltage of said transistor (this is inherent characteristics of floating gate transistor); and

a programming gate (control gate 2 formed on the control oxide and having dark region) adjacent said floating gate, wherein said floating gate is between said programming gate and said channel region.

Regarding claim 37, She discloses the transistor further comprising source and drain regions at ends of said channel region, wherein said channel region comprises the middle portion of the fin structure and said source and drain regions comprise end portions of said fin structure. See figs. 8-11.

Regarding claim 38, She discloses the transistor wherein said floating gate is electrically insulated from other structures. See figs. 10-11.

6. Claim(s) 1, 3, 4, 7, 8, 10, 11, 14, 29, and 34 stand rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,107,141 to Hsu et al.

Regarding claim 1, Hsu discloses a multiple-gate transistor, as shown in figs. 1, 2, and 9, comprising:

a channel region (between source 20 and drain 20;

a logic gate 120 adjacent a first side (left side) of said channel region;

a floating gate 130 adjacent a second side (right side) of said channel region, wherein said first side is opposite said second side; and

a programming gate 140 adjacent said floating gate 130, wherein said floating gate 130 is between said programming gate 140 and said channel region.

Regarding claim 8, Hsu discloses a multiple-gate transistor, as shown in figs. 1, comprising:

a channel region; source and drain regions 30/20 at ends of said channel region;

a gate oxide 232 on a first side (left side) of said channel region;

a logic gate 120 adjacent said first gate oxide 232, wherein said gate oxide 232 is between said logic gate 120 and said channel region;

a first insulator 235 on a second side (right side) of said channel region, wherein said second side of said channel region is opposite said first side;

a floating gate 130 adjacent said first insulator 235, wherein said first insulator 235 is between said floating gate 130 and said channel region;

a second insulator 237 adjacent said floating gate 130; and

a programming gate 140 adjacent said second insulator 237, wherein said second insulator 237 is between said programming gate 140 and said floating gate 130.

Regarding claims 3 and 10, Hsu discloses the transistor wherein voltage in said logic gate 120 causes said transistor to switch on and off. Col. 1 line 66 to col. 2, line 1 state(s) that logic or select gate 120 serves the standard electrical function of permitting access to the cell. Thus, controlling the voltage applied to the logic gate 120 would control the access to the cell, or would turn the cell on and off.

Regarding claims 4 and 11, Hsu discloses the transistor wherein charge in said floating gate 130 adjusts the threshold voltage of said transistor. This is inherent since a charge in the floating gate 130 would create an electric field in the insulator 235; therefore, such charge would effect the threshold voltage of the transistor.

Regarding claims 7 and 14, Hsu discloses the transistor wherein said floating gate 130 is electrically insulated from other structures. See fig. 1.

Regarding claim 29, Hsu discloses a multiple-gate transistor, as shown in figs. 1, 2, and 9, comprising:

a channel region (on top surface of substrate 10, between drain region 20 and source region 30);

a logic gate 120 adjacent a first side (left or source side) of said channel, wherein voltage in said logic gate causes said transistor to switch on and off (col. 1 line 66 to col. 2, line 1 state(s) that logic or select gate 120 serves the standard electrical function of

permitting access to the cell; thus, controlling the voltage applied to the logic gate 120 would control the access to the cell, or would turn the cell on and off);

a floating gate 130 adjacent a second side (right or drain side) of said channel region, wherein said first side (source side) is opposite said second side (drain side), and wherein charge in said floating gate 130 adjusts the threshold voltage of said transistors (this is inherent characteristics of floating gate transistor); and

a programming gate 140 adjacent said floating gate 130, wherein said floating gate 130 is between said programming gate 140 and said channel region.

Regarding claim 34, Hsu discloses the transistor wherein said floating gate 130 is electrically insulated from other structures. See fig. 1.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim(s) 2, 9, 31, and 36 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent Application Publication No. 2005/0242391 by She et al.

Regarding claims 2, 9, 31, and 36, She discloses the transistor comprising all claimed limitations, including a gate oxide (tunnel oxide) between said channel region and said logic gate and a first insulator between said channel region and said floating gate, except for expressly teaching that the first insulator is thicker than the gate oxide.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the thicknesses of the gate oxide layer and the first insulating layer are significantly depending on (the dielectric constant of) the materials being used to form each of them; and selecting a known material on the basis of its suitability for the intended use is just within the general skill of a worker in the art. In re Leshin, 125 USPQ. Furthermore, a modification to have a thickness of one layer to be thicker or thinner than that of the other layer would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Conclusion

9. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571)272-1907. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Douglas W. Owens 8/6/06

DOUGLAS W. OWENS
PRIMARY EXAMINER

Dao H. Nguyen
Art Unit 2818
July 27, 2006